IN THE CLAIMS

1. (Currently Amended) A processing system comprising:

first processing circuitry for performing a first function;

first reassembly circuitry, associated with the first processing circuitry, for reassembling segments of received packets into reassembled packets, the segments to be reassembled being related to the first function;

first memory circuitry, ~~coupled to~~ associated with the first processing circuitry, for storing ~~received~~ the packets reassembled by the first reassembly circuitry, ~~at least a portion of~~ wherein the reassembled packets stored by the first memory circuitry ~~being usable~~ are used by the first processing circuitry in accordance with the first function;

at least second processing circuitry for performing a second function;

at least second reassembly circuitry, associated with the second processing circuitry, for reassembling at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembled packets, the segments to be reassembled being related to the second function; and

at least second memory circuitry, ~~coupled to~~ associated with the second processing circuitry, for storing ~~at least a portion of the same~~ the packets reassembled by the second reassembly circuitry, such that at least a portion of the reassembled packets stored in the first memory circuitry and the second memory circuitry are the same, ~~at least a portion of~~ wherein the reassembled packets stored in the second memory circuitry ~~being usable~~ are used by the second processing circuitry in accordance with the second function.

2. (Currently Amended) The system of claim 1 wherein the first processing circuitry, the first reassembly circuitry, the first memory circuitry, the second processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on ~~the same~~ an integrated circuit.

3. (Currently Amended) The system of claim 1 wherein the first processing circuitry, the first reassembly circuitry and the first memory circuitry are implemented on a first integrated circuit, and the second processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on a second integrated circuit.

4. (Currently Amended) The system of claim 1 wherein the first function and the second function are performed ~~in accordance with~~ by ~~the same~~ an integrated circuit.

5. (Currently Amended) The system of claim 1 wherein the first function and the second function are performed ~~in accordance with~~ by different integrated circuits.

6. (Currently Amended) The system of claim 1 wherein the first processing circuitry, the first reassembly circuitry and the first memory circuitry comprise a network processor.

7. (Original) The system of claim 6 wherein the first function comprises a packet classifying operation.

8. (Currently Amended) The system of claim 1 wherein the second processing circuitry, the second reassembly circuitry and the second memory circuitry comprise a traffic manager.

9. (Original) The system of claim 8 wherein the second function comprises a packet scheduling operation.

10. (Canceled).

11. (Currently Amended) The system of claim ~~10~~ 1 further comprising parsing circuitry, coupled to the first reassembly circuitry and the second reassembly circuitry, for parsing information from the received packets for use by the first reassembly circuitry and the second reassembly circuitry in respectively reassembling the packets.

12. (Currently Amended) The system of claim 10 wherein the packet~~subsets~~ segments are cells.

13. (Original) The system of claim 1 wherein the first processing circuitry and the second processing circuitry operate in a packet switching device.

14. (Original) The system of claim 13 wherein the first processing circuitry and the second processing circuitry operate between a packet network interface and a switch fabric of the packet switching device.

15. (Currently Amended) A method for use in a processing system wherein the processing system is responsive to packets, the method comprising the steps of:

reassembling ~~subsets~~ segments of received packets into reassembled packets in a first reassembler, wherein the segments being reassembled are related to a first function; and

storing the reassembled packets in a first memory, ~~at least a portion of~~ the reassembled packets stored by the first memory ~~being usable~~ are used by a first processor in accordance with ~~a~~ the first function;

wherein at least a portion of the ~~subsets~~ segments of received packets reassembled by the first reassembler may be reassembled in at least a second reassembler for storage in at least a second memory usable by at least a second processor in accordance with a second function, such that at least a portion of the reassembled packets stored in the first memory and the second memory are the same.

16. (Currently Amended) The method of claim 15 wherein the first reassembler, the first processor, the first memory, the second reassembler, the second processor and the second memory are implemented on ~~the same~~ an integrated circuit.

17. (Original) The method of claim 15 wherein the first reassembler, the first processor and the first memory are implemented on a first integrated circuit, and the second reassembler, the second processor and the second memory are implemented on a second integrated circuit.

18. (Currently Amended) Apparatus for use in a processing system wherein the processing system is responsive to packets, the apparatus comprising:

a first memory; and

a first processor operative to: (I) reassemble ~~subsets~~ segments of received packets into reassembled packets, wherein the segments being reassembled are related to a first function; and (ii) cause the storage of the reassembled packets in the first memory, ~~at least a portion of~~ the

reassembled packets stored by the first memory ~~being usable~~ are used in accordance with ~~a~~ the first function;

wherein at least a portion of the ~~subsets~~ segments of received packets reassembled by the first ~~reassembler~~ processor may be reassembled by at least a second processor for storage in at least a second memory usable in accordance with a second function, such that at least a portion of the reassembled packets stored in the first memory and the second memory are the same.

19. (Currently Amended) The apparatus of claim 18 wherein the first processor and the first memory, the second processor and the second memory are implemented on ~~the same~~ an integrated circuit.

20. (Original) The apparatus of claim 18 wherein the first processor and the first memory are implemented on a first integrated circuit, and the second processor and the second memory are implemented on a second integrated circuit.